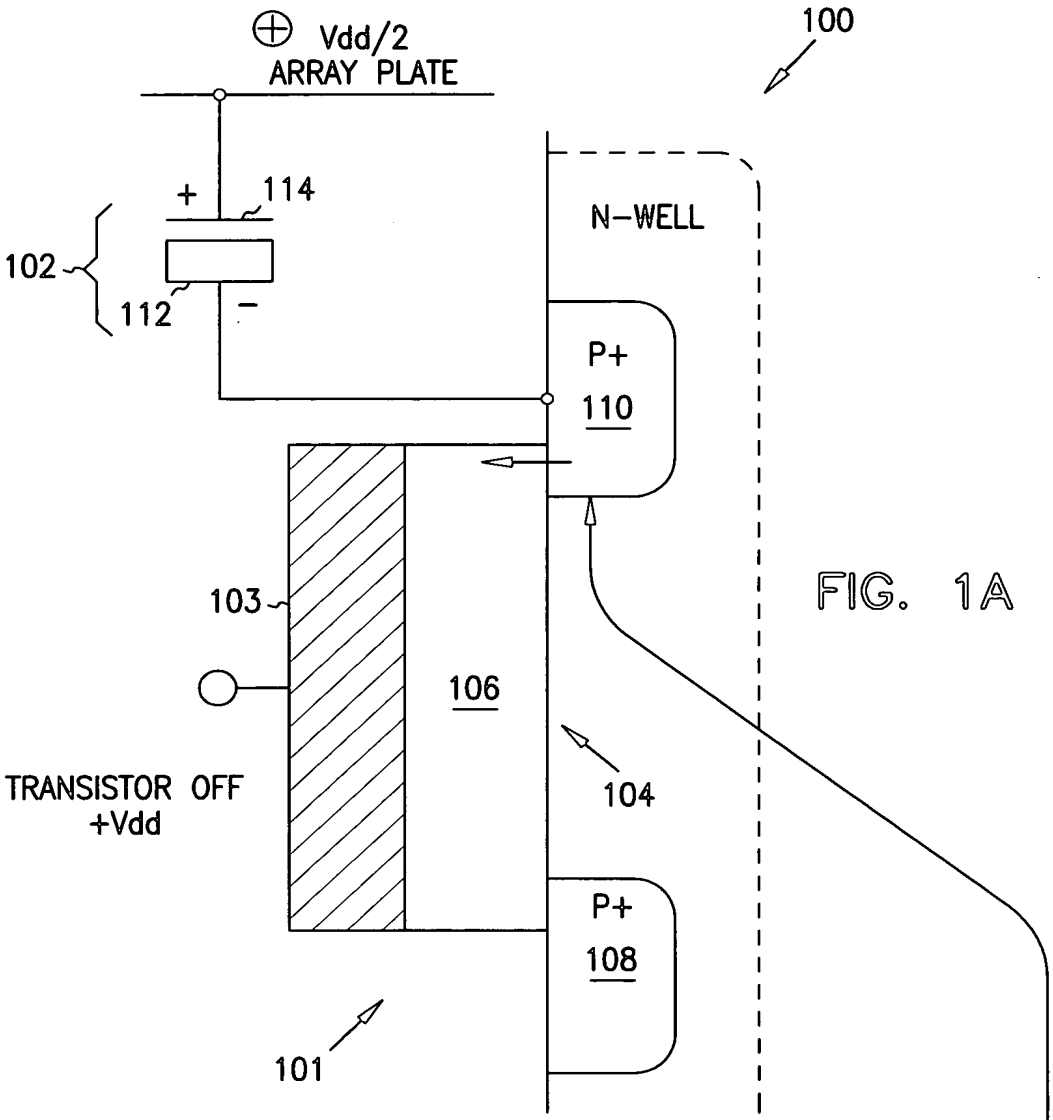


FIG. 1A

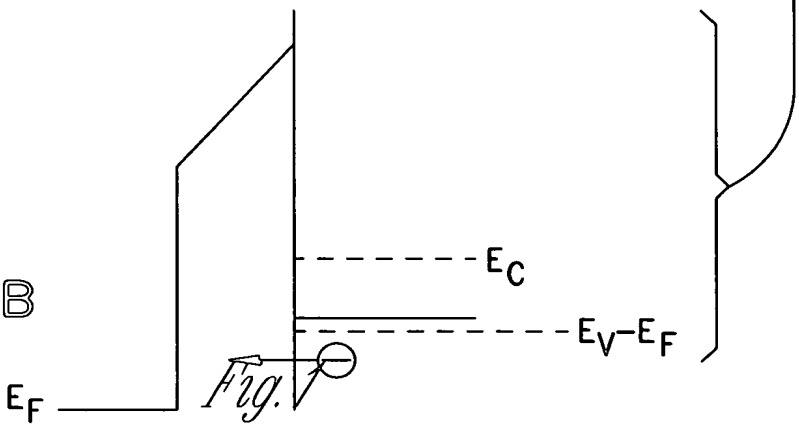
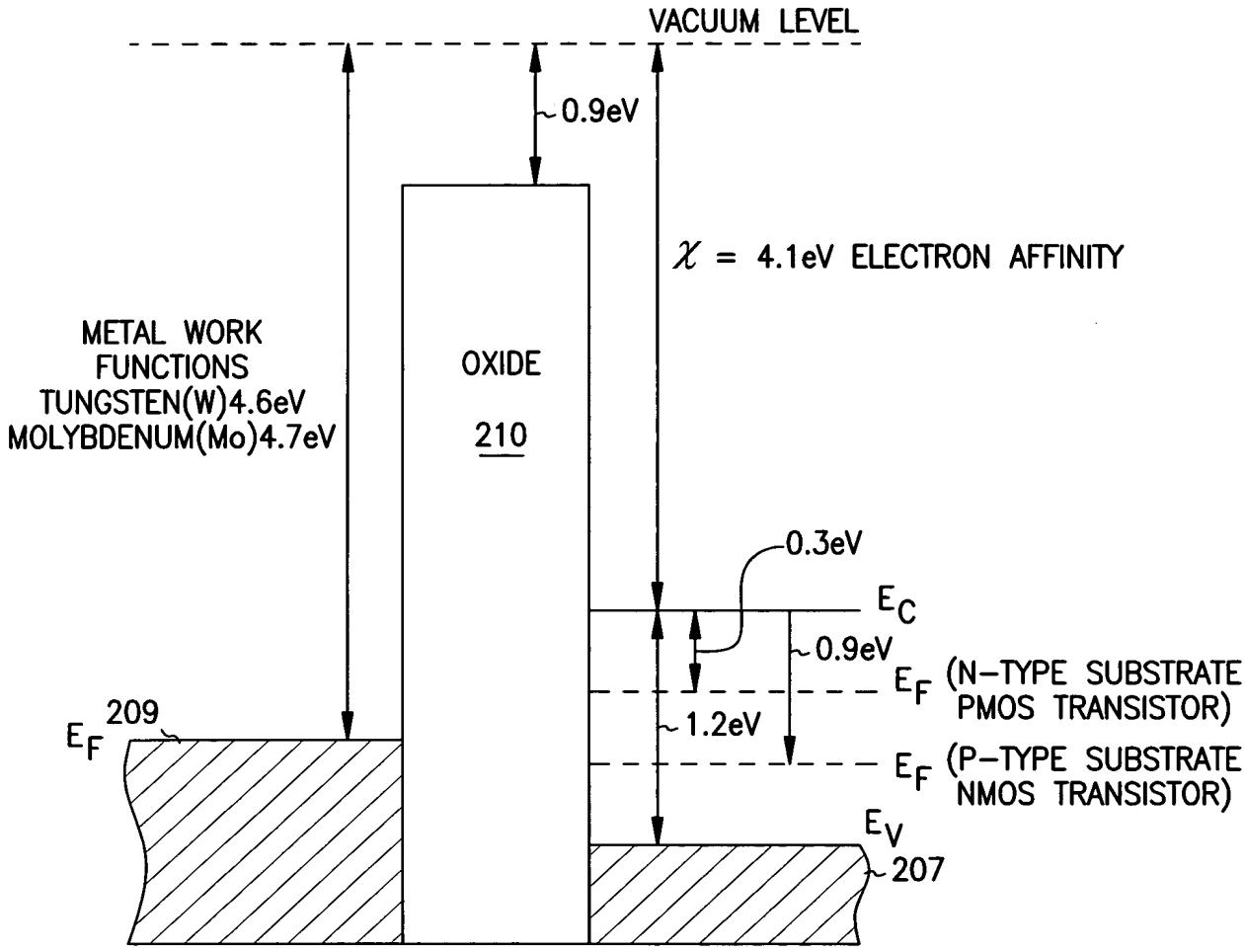


FIG. 1B

Fig. 1



"MID-GAP" METALS USED FOR OPTIMIZING NMOS AND PMOS TRANSISTOR THRESHOLDS VOLTAGES; METAL SEMICONDUCTOR WORK FUNCTION DIFFERENCES

NMOS: Φms = 4.7−5.0eV = −0.3V

PMOS: Φms = 4.7−4.4eV = +0.3V

FIG. 2
(PRIOR ART)

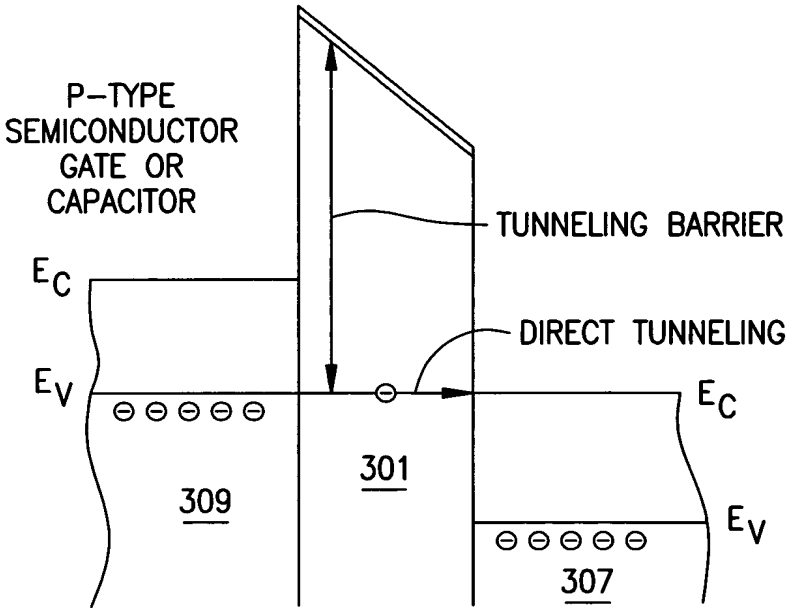

P–TYPE
SEMICONDUCTOR
GATE OR
CAPACITOR
TUNNELING BARRIER
E_C
DIRECT TUNNELING
E_V
E_C
301
309
E_V
307

FIG. 3A

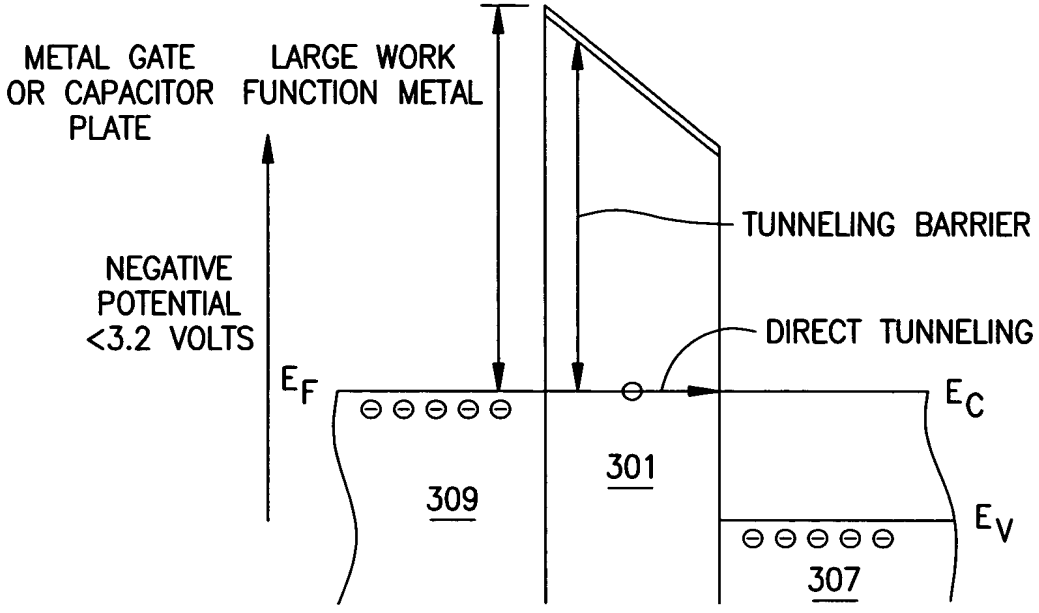

METAL GATE
OR CAPACITOR
PLATE
LARGE WORK
FUNCTION METAL
TUNNELING BARRIER
NEGATIVE
POTENTIAL
<3.2 VOLTS
DIRECT TUNNELING
E_F
E_C
301
309
E_V
307

FIG. 3B

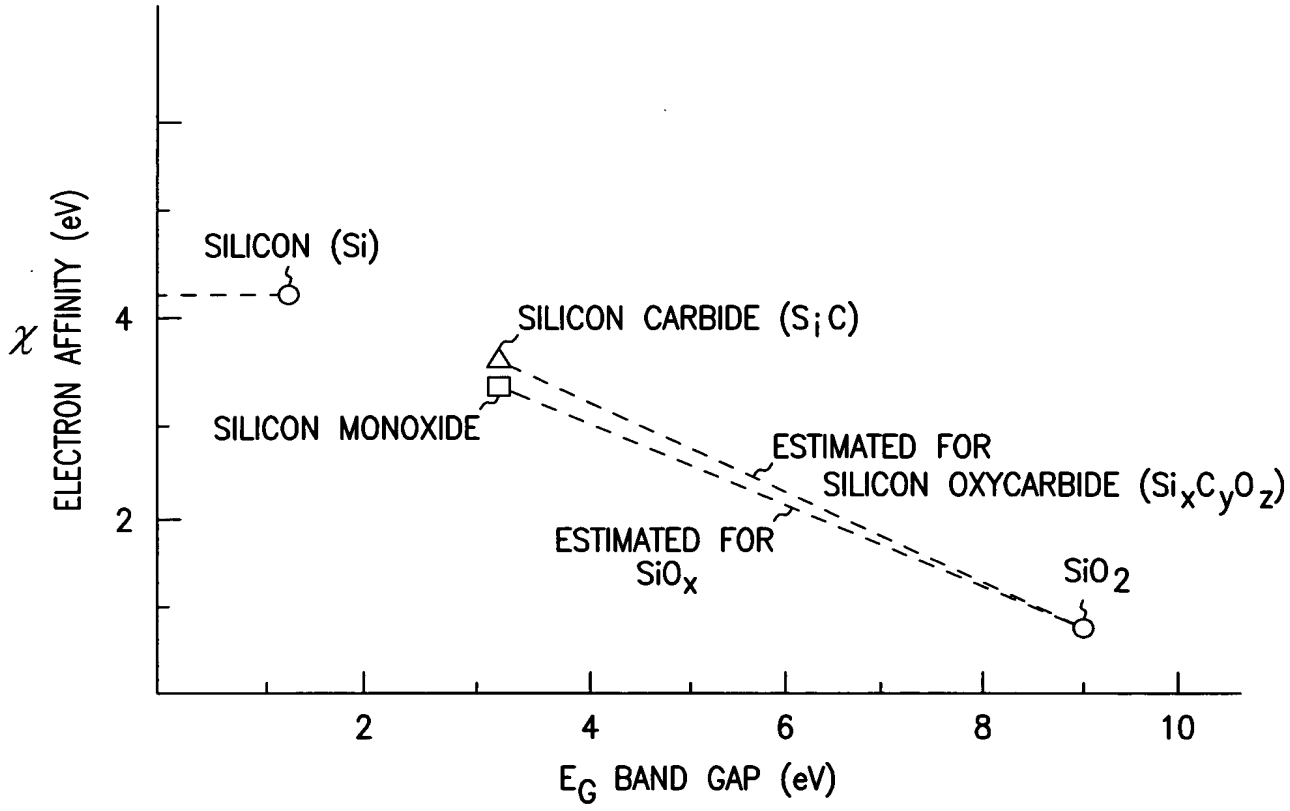

ELECTRON AFFINITY (eV)
χ
4
2
SILICON (Si)
SILICON CARBIDE (SiC)
SILICON MONOXIDE
ESTIMATED FOR
SILICON OXYCARBIDE ($Si_xC_yO_z$)
ESTIMATED FOR
SiO_x
SiO_2
2
4
6
8
10
E_G BAND GAP (eV)

FIG. 4

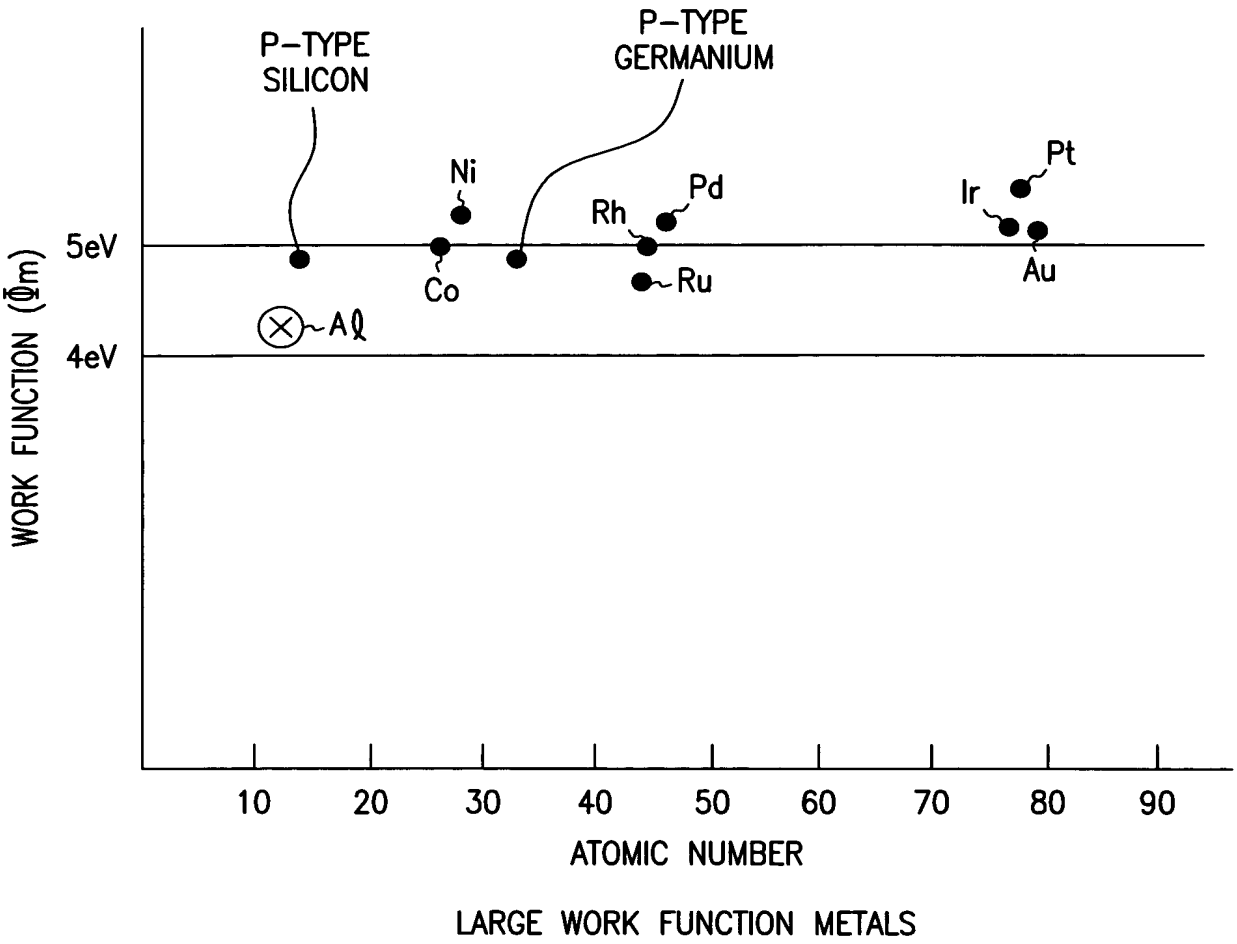

P-TYPE SILICON
P-TYPE GERMANIUM
Ni
Co
Rh
Pd
Ru
Ir
Pt
Au
Al
5eV
4eV
WORK FUNCTION (Φm)
10
20
30
40
50
60
70
80
90
ATOMIC NUMBER
LARGE WORK FUNCTION METALS

FIG. 5

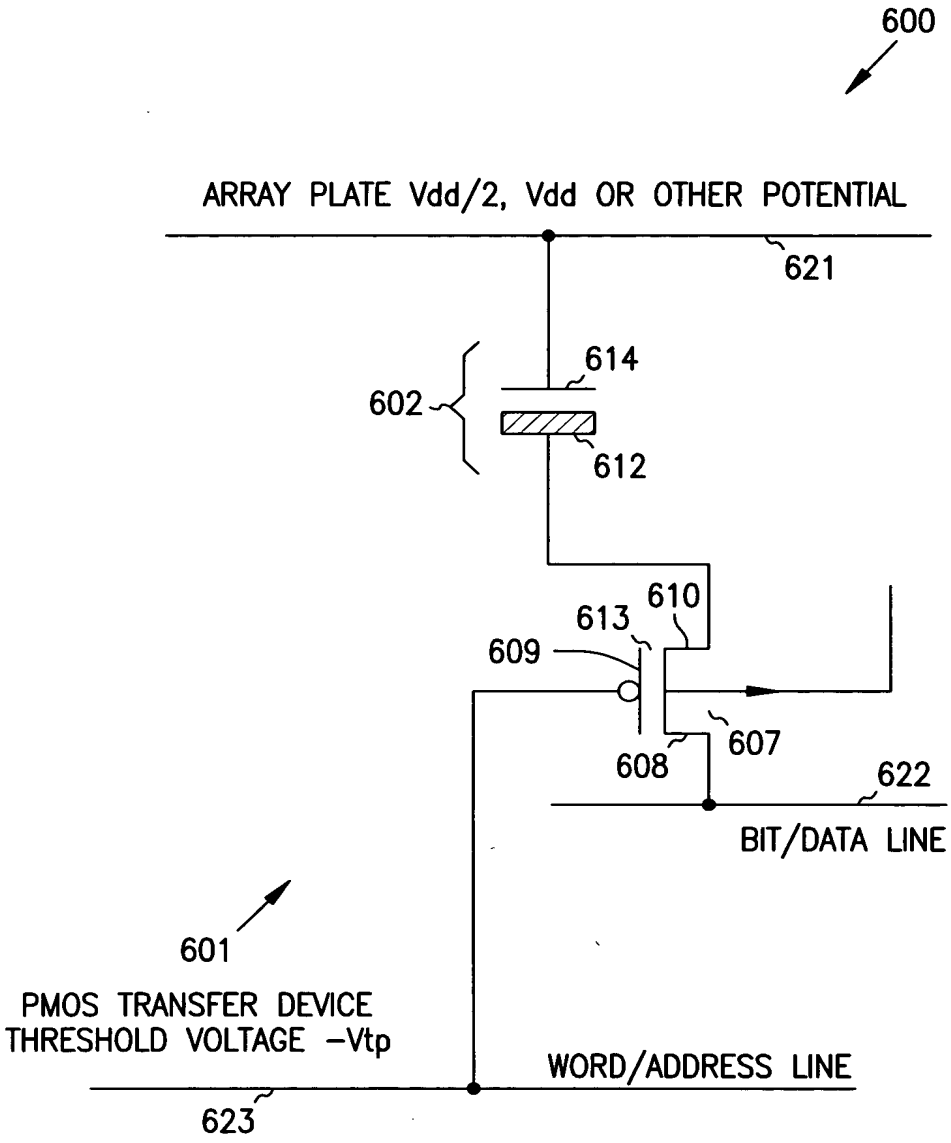

600
ARRAY PLATE Vdd/2, Vdd OR OTHER POTENTIAL
621
614
602
612
610
613
609
607
608
622
BIT/DATA LINE
601
PMOS TRANSFER DEVICE
THRESHOLD VOLTAGE -Vtp
WORD/ADDRESS LINE
623

FIG. 6

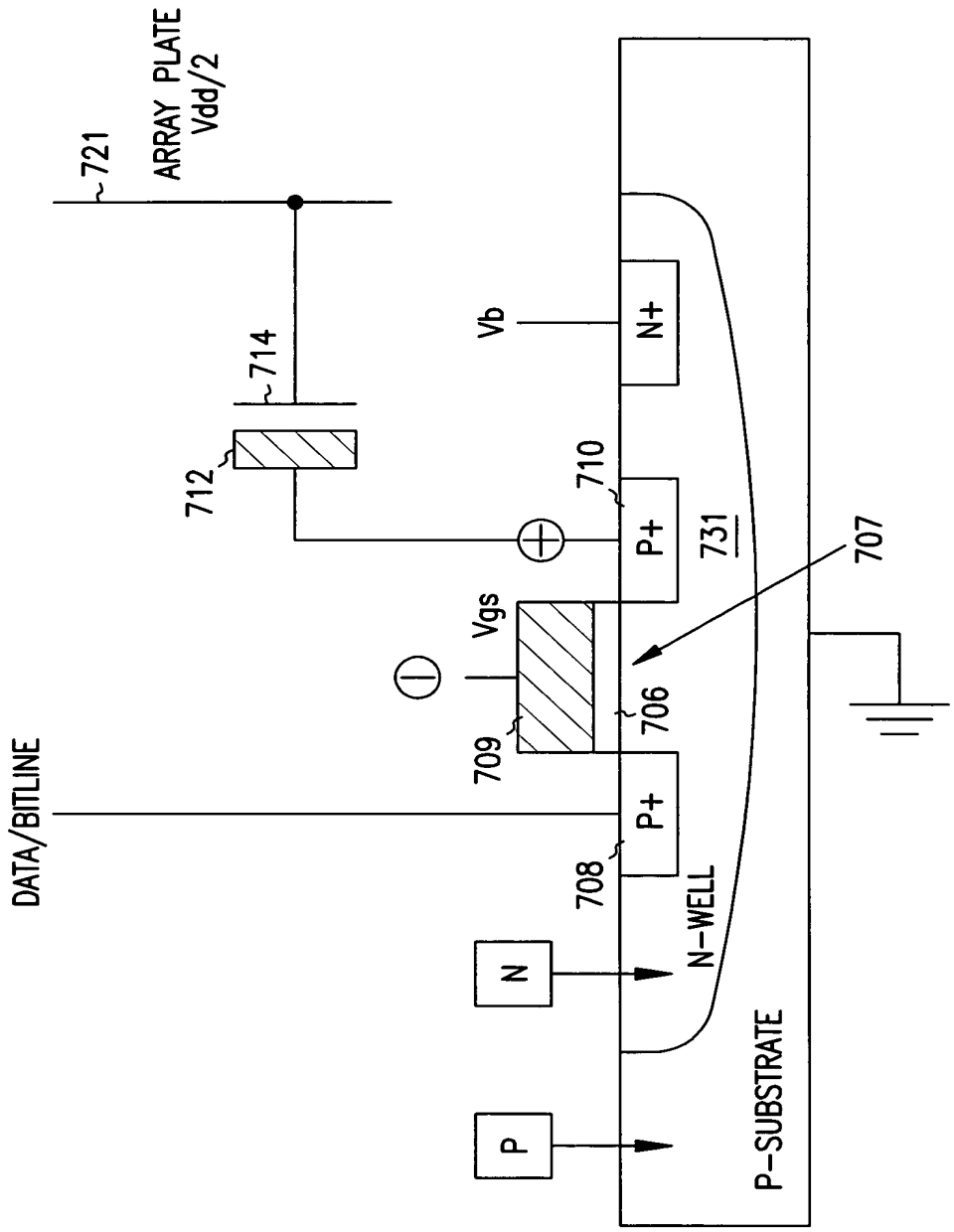

721
ARRAY PLATE
Vdd/2
714
712
Vb
N+
710
P+
731
707
Vgs
706
709
DATA/BITLINE
P+
708
N-WELL
N
P
P-SUBSTRATE

FIG. 7